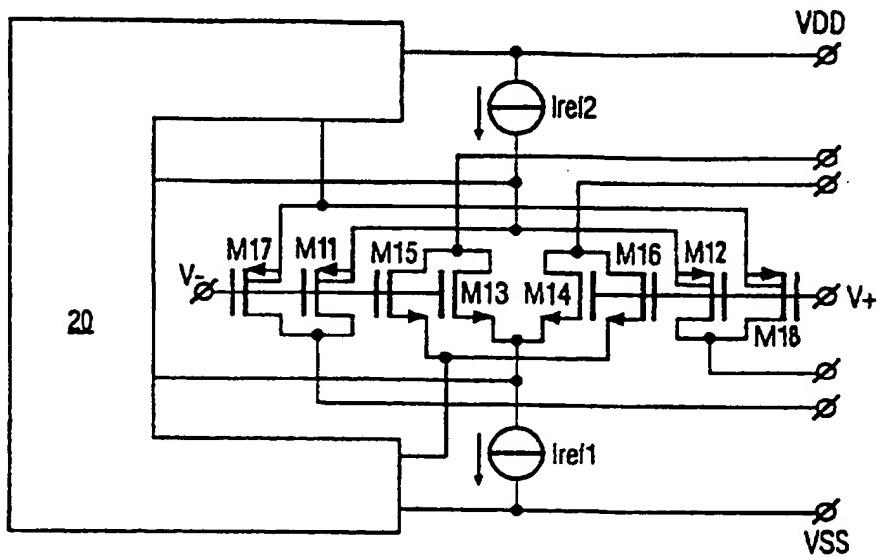




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :	A2	(11) International Publication Number: WO 96/34451
H03F 3/45		(43) International Publication Date: 31 October 1996 (31.10.96)
(21) International Application Number:	PCT/IB96/00179	(81) Designated States: JP, KR, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).
(22) International Filing Date:	7 March 1996 (07.03.96)	
(30) Priority Data:		Published
08/430,517	27 April 1995 (27.04.95)	Without international search report and to be republished upon receipt of that report.
(71) Applicant:	PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).	
(71) Applicant (for SE only):	PHILIPS NORDEN AB [SE/SE]; Kottbygatan 5, Kista, S-164 85 Stockholm (SE).	
(72) Inventors:	HOGERVORST, Ronald; Koperwijkstraat 100, NL-2251 NZ Voorschoten (NL). HULSING, Johan, Hendrik; 't Wandt 10, NL-2636 HD Schipluiden (NL). TERO, John, P.; 19234 Bellwood Drive, Saratoga, CA 95070 (US).	
(74) Agent:	HESSELMANN, Gerardus, J., M.: Internationaal Octrooibureau B.V., P.O. Box 220, NL-5600 AE Eindhoven (NL).	

(54) Title: RAIL-TO-RAIL INPUT STAGES WITH g_m -CONTROL BY MULTIPLE INPUT PAIRS

(57) Abstract

A transconductance (g_m) control circuit for bipolar or CMOS rail-to-rail input stages is provided. The g_m is controlled by the use of multiple input pairs and can be used in CMOS or bipolar technology. In CMOS the g_m -control works regardless of the operating region of the MOS transistor, whether it is weak, moderate or strong inversion.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AM	Armenia	GB	United Kingdom	MW	Malawi
AT	Austria	GE	Georgia	MX	Mexico
AU	Australia	GN	Guinea	NE	Niger
BB	Barbados	GR	Greece	NL	Netherlands
BE	Belgium	HU	Hungary	NO	Norway
BF	Burkina Faso	IE	Ireland	NZ	New Zealand
BG	Bulgaria	IT	Italy	PL	Poland
BJ	Benin	JP	Japan	PT	Portugal
BR	Brazil	KE	Kenya	RO	Romania
BY	Belarus	KG	Kyrgyzstan	RU	Russian Federation
CA	Canada	KP	Democratic People's Republic of Korea	SD	Sudan
CF	Central African Republic	KR	Republic of Korea	SE	Sweden
CG	Congo	KZ	Kazakhstan	SG	Singapore
CH	Switzerland	LI	Liechtenstein	SI	Slovenia
CI	Côte d'Ivoire	LK	Sri Lanka	SK	Slovakia
CM	Cameroon	LR	Liberia	SN	Senegal
CN	China	LT	Lithuania	SZ	Swaziland
CS	Czechoslovakia	LU	Luxembourg	TD	Chad
CZ	Czech Republic	LV	Lvavia	TG	Togo
DE	Germany	MC	Monaco	TJ	Tajikistan
DK	Denmark	MD	Republic of Moldova	TT	Trinidad and Tobago
EE	Estonia	MG	Madagascar	UA	Ukraine
ES	Spain	ML	Mali	UG	Uganda
FI	Finland	MN	Mongolia	US	United States of America
FR	France	MR	Mauritania	UZ	Uzbekistan
GA	Gabon			VN	Viet Nam

Rail-to-rail input stages with g_m -control by multiple input pairs.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to controlling the transconductance (g_m) of the input stages of an operational amplifier to improve performance and enhance applications.

More particularly, the invention relates to a circuit for controlling the transconductance (g_m) of the an input stage of an operational amplifier (opamp), the input stage having at least an N-channel and a P-channel input differential pair of transistors each having a tail current, the opamp having a common-mode input voltage range including low, intermediate, and high common-mode input voltages.

10

The Prior Art

Such a circuit is known from U.S. Patent No. 4,555,673 to Huijsing et al., which discloses a differential amplifier with rail-to-rail input capability and controlled transconductance (g_m). The method employed for controlling the transconductance uses current control or current switches to steer at least part of the supply current away from at least one of the differential portions of the input stage when the common mode voltage is in at least one part of the supply range.

Other methods for controlling the transconductance (g_m) of the input stages of operational amplifiers with CMOS technology use square root circuits, three times current 20 mirrors, and current switches in order to maintain the g_m of the input stages substantially constant. (Botma, J.H., et al., "A low-voltage CMOS operational amplifier with rail-to-rail constant-gm input stage and class-AB rail-to-rail output stage", Proceeding ISCAS93, pp.1314-1317; Hogervorst, R. et al., "CMOS low-voltage operational amplifiers with constant-gm rail-to-rail input stage", Proceedings ISCAS92, pp.2876-2879; R. Hogervorst, 25 J.P.Tero, R.G.H. Rschauzier, J.H. Huijsing, "A compact power-efficient rail-to-rail input/output amplifier for VLSI cell libraries". in Digest ISSCC94, Feb 1994.)

The main drawbacks of these existing g_m -controlled rail-to-rail input stages can be found in CMOS technology. Specifically, they are not appropriate for MOS complementary input stages operating in moderate inversion. That is, the transition region

between weak and strong inversion. An input stage is frequently biased in moderate inversion because it is a good compromise between a low-offset and a high slew rate.

Another drawback which occurs particularly in CMOS input stages operating in strong inversion, is that the common-mode output currents are 4 times larger at the outer 5 parts of the common-mode input range compared to the intermediate part of the common-mode input range.

Furthermore, the g_m of a CMOS complementary input stage can only be varied over a small range which limits the applicability for which the circuit may be used. In opamps intended for VLSI cell libraries it is often required that the g_m of the input stage be 10 adapted over a large range, so that the specification of the opamp can easily be changed to the need of the specific application.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a circuit for maintaining the 15 transconductance (g_m) of an input stage of an operational amplifier constant over a large operating range.

Another object of the invention is to provide a circuit for controlling the g_m of the input stage of an operational amplifier using either bipolar or CMOS technology.

It is another object of the invention to provide a circuit for g_m -control with 20 CMOS technology that operates efficiently regardless of the operating region of the MOS transistor.

Yet another object of the invention is to provide a circuit for g_m -control that reduces the power dissipation of CMOS input stages biased in the strong inversion operating region.

Another object of the invention is to provide a circuit for g_m -control that is 25 suitable for CMOS input stages operating in moderate inversion.

It is a further object of the invention to provide a circuit for g_m -control that avoids a waste of power in a folded cascoded summing circuit by maintaining the sum of the tail currents of the input pairs constant.

According to the invention the circuit as specified in the opening paragraph is 30 characterized in that the circuit comprises:

an additional N-channel differential pair of transistors coupled to the N-channel input pair;

an additional P-channel differential pair of transistors coupled to the P-channel

input pair; and

control means coupled to both of said additional input pairs for activating one of said additional input pairs in response to low and high common-mode input voltages.

5 BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and features of the present invention will become apparent from the following detailed description considered in connection with the accompanying drawings which disclose an embodiment of the present invention. It should be understood, however, that the drawings are designed for the purpose of illustration only and not as a definition of the limits of the invention.

In the drawings, wherein similar reference characters denote similar elements throughout the several views:

Fig. 1 is a schematic diagram of the input stage of an operational amplifier of the prior art;

15 Fig. 2A is a partial block diagram of the controlled g_m input stage according to the invention;

Fig. 2B is a schematic diagram of the controlled g_m input stage according to the invention;

20 Fig. 3A is graphical representation of the transconductance versus the common mode input range in weak inversion according to the invention; and

Fig. 3B is a graphical representation of the transconductance versus the common mode input range in strong inversion according to the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

25 Fig. 1 shows an example of an input stage of an operational amplifier of the prior art. As shown, the input stage has a rail-to-rail common-mode input range which can be composed of two complementary differential input pairs. The input stage consists of an N-channel input pair, M13-M14, and a P-channel input pair, M11-M12. The common-mode input voltage range for such an input stage can be divided into three parts: (1) Low common-mode input voltages (only the P-channel input pair operates); (2) Intermediate common-mode input voltages; (both the P-channel and N-channel input pair operate); and, (3) High common-mode input voltages (only the N-channel input pair operates).

When the common-mode input voltage moves from one part of the common-mode input range into another, the transconductance (g_m) changes with a factor of two.

Thus, since the unity-gain frequency of an amplifier is proportional to the g_m of the input stage, changes in the g_m impedes an optimal frequency compensation. Therefore, in order to obtain optimal frequency compensation over the whole common-mode input range, the g_m of the input stage has to be constant.

5

Fig. 2A shows the differential input stage M11-M14 with the two additional input pairs, M15-M16, and M17-M18, and control circuit 20. Control circuit 20 regulates the activation of the additional input pairs M15-M16, and M17-M18 in response to the change of the common-mode input voltage.

In the intermediate part of the common-mode input range, the P-channel input pair M11-M12 and the N-channel input pair M13-M14 are active. At the outer parts of the common-mode input range, control circuit 20 places one of the additional input pairs in parallel with the active input pair. As a result, the g_m is increased by a factor of 2 at the outer parts of the common-mode input range. This principle works regardless of the technology used, whether it is bipolar or CMOS. Furthermore, it is independent of the operating region of the transistor, whether it is weak, moderate, or strong inversion.

10

Fig. 2B shows a specific schematic example of the input stage where control circuit 20 includes two current switches M109 and M113, two current mirrors, M110-M111, and M114-M115, and threshold voltage sources Vb1 and Vb2. In the intermediate part of the common-mode input range, the P-channel input pair M11-M12 and the N-channel input pair M13-M14 are active.

15

If low common-mode input voltages are applied, only the P-channel input pair, M11-M12 operates. The N-channel current switch M109 conducts, while the P-channel current switch M113 is off. The N-channel current switch M109 takes away the tail current of the N-channel input pair M13-M14, and feeds it through current mirror M110-M111, into the additional P-channel input pair M17-M18. Since the additional input pair M17-M18 is in parallel with the P-channel input pair M11-M12, the total transconductance is equal to $2g_m$.

20

If intermediate common-mode input voltages are applied, both the P-channel input pair M11-M12, as well as the N-channel input pair M13-M14, operate. In this range, both current switches M109 and M113 are off. As a consequence, the N-channel and the P-channel input pair have a tail current of I_{ref} . Thus, assuming that the g_m of the P-channel and the N-channel input pair is equal, the total transconductance of the complementary input stage is equal to $2g_m$.

If high common-mode input voltages are applied, only the N-channel input pair M13-M14 operates. The P-channel current switch M113 conducts, while the N-channel

current switch M109 is off. The P-channel current switch M113 takes away the tail current of the P-channel input pair M11-M12 and directs it, via the current mirror M114-M115, into the additional N-channel input pair M15-M16. Since the additional input pair is in parallel with N-channel input pair M13-M14, the total transconductance of the input stage is equal to 5 $2g_m$.

It should be noted that the sum of the tail-currents is constant over the common-mode input range. Especially for CMOS input stages operating in strong inversion, this results in a reduction of the power consumption. Thus, the summing circuit, which follows the input stage, can be biased at a current which is two times smaller compared to existing 10 technology.

FIGS. 3A and 3B show a graphical representation of the normalized transconductance (g_m) as a function of the common-mode input range for the circuit according to the invention. Fig. 3a shows that the g_m is constant over the common-mode input range when a bipolar or a CMOS input stage biased in weak inversion is used. Fig. 15 3B shows that the g_m is also constant for a CMOS input stage operating in strong inversion, except for two takeover regions 30 and 32 where the transconductance varies about 20%. In these take-over regions, the current through current switches M109 and M113 varies from 0 to I_{ref} or vice versa.

Control circuit 20 (Fig. 2A) can be adapted to further reduce the variation in 20 the transconductance in take over regions 30 and 32. For example, by changing the value of threshold voltage sources Vb1 and Vb2 and the specific values of some of the components in control circuit 20, the g_m in takeover regions 30 and 32 can be made smaller.

When common-mode input voltages are applied at the lower end of the takeover 25 region 30 to the circuit of Fig. 2B, increasing the width-to-length ratio of M110 will lower the transport of current in relation to M111. Thus, the transport ratio of mirror M110, M111 is now less than 1 and the g_m of the takeover region 30 is diminished. To correct the g_m again at the higher end of the take over region, an increase in current can be achieved by adding a resistor in series with the source of M111. The same principles apply for high 30 common-mode input voltages and the respective components M114 and M115 associated therewith.

In another embodiment of the invention (not shown), the g_m can be made more constant by adding more additional input pairs to the input stage of the opamp with spread spacing of the multiple take over regions.

While two embodiments of the present invention has been shown and described,

it is to be understood that many changes and modifications may be made thereunto without departing from the spirit and scope of the invention as defined in the appended claims.

CLAIMS:

1. A circuit for controlling the transconductance (gm) of the an input stage of an operational amplifier (opamp), the input stage having at least an N-channel (M13, M14) and a P-channel (M11, M12) input differential pair of transistors each having a tail current, the opamp having a common-mode input voltage range including low, intermediate, and high common-mode input voltages, characterized in that the circuit comprises:

an additional N-channel differential pair (M15, M16) of transistors coupled to the N-channel input pair;

an additional P-channel differential pair (M17, M18) of transistors coupled to the P-channel input pair; and

10 control means (20) coupled to both of said additional input pairs for activating one of said additional input pairs in response to low and high common-mode input voltages.

2. The circuit according to claim 1 wherein, said additional N-channel input pair (M15, M16) is connected to the N-channel input pair (M13, M14) of the input stage of the opamp in parallel, and said additional P-channel input pair (M17, M18) is connected to the 15 P-channel input pair (M11, M12) of the input stage of the opamp in parallel.

3. The circuit according to claim 2, wherein said control means (20) further comprises:

an N-channel current switch (M109) coupled to the N-channel input pair (M13, M14) and said additional N-channel input pair (M15, M16);

20 a first current mirror (M110, M111) having an input coupled to said N-channel current switch (M109) and an output coupled to said additional P-channel input pair (M17, M18);

a P-channel current switch (M113) coupled to the P-channel input pair (M11, M12) and said additional P-channel input pair (M17, M18); and

25 a second current mirror (M114, M115) having an input coupled to said P-channel current switch (M113) and an output coupled to said additional N-channel input pair (M15, M16).

4. The circuit according to claim 3, wherein when low common mode voltages are applied to the input stage of the opamp, said N-channel current switch (M109) conducts the

tail current of the N-channel input pair (M13, M14) into said additional P-channel input pair (M17, M18) via said first current mirror (M110, M111) thereby controlling and maintaining the transconductance (g_m) of the input stage at a constant value.

5. The circuit according to claim 3, wherein when high common-mode voltages are applied to the input stage of the opamp, said P-channel current switch (M113) conducts the tail current of the P-channel input pair (M11, M12) into said additional N-channel input pair (M15, M16) via said second current mirror (M114, M115) thereby controlling and maintaining the transconductance (g_m) of the input stage at a constant.
6. The circuit according to claim 3, wherein the input stage of the opamp has 10 takeover regions having variable transconductance values, and whereby said control means (20) are operative to reduce the transconductance variation of the takeover regions of the input stage of the opamp.

1/3

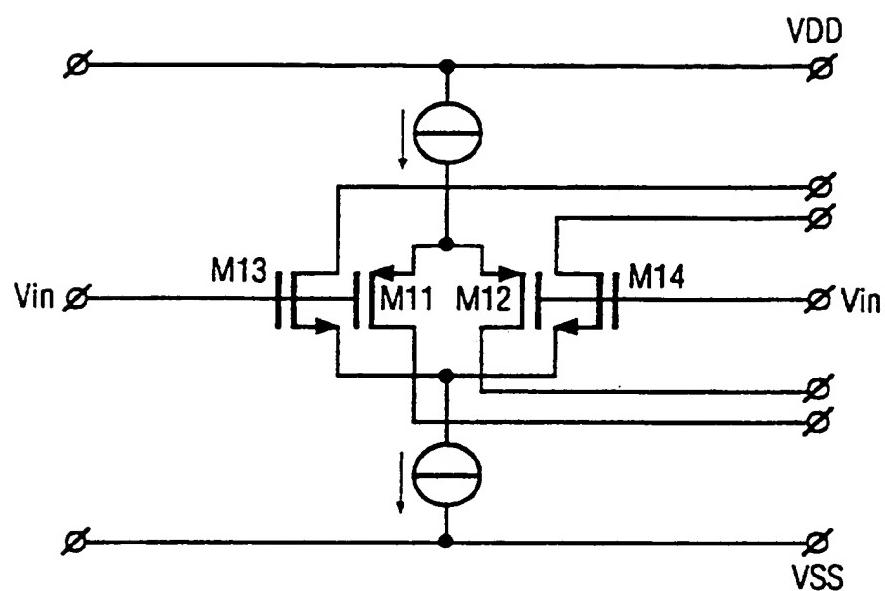


FIG. 1

2/3

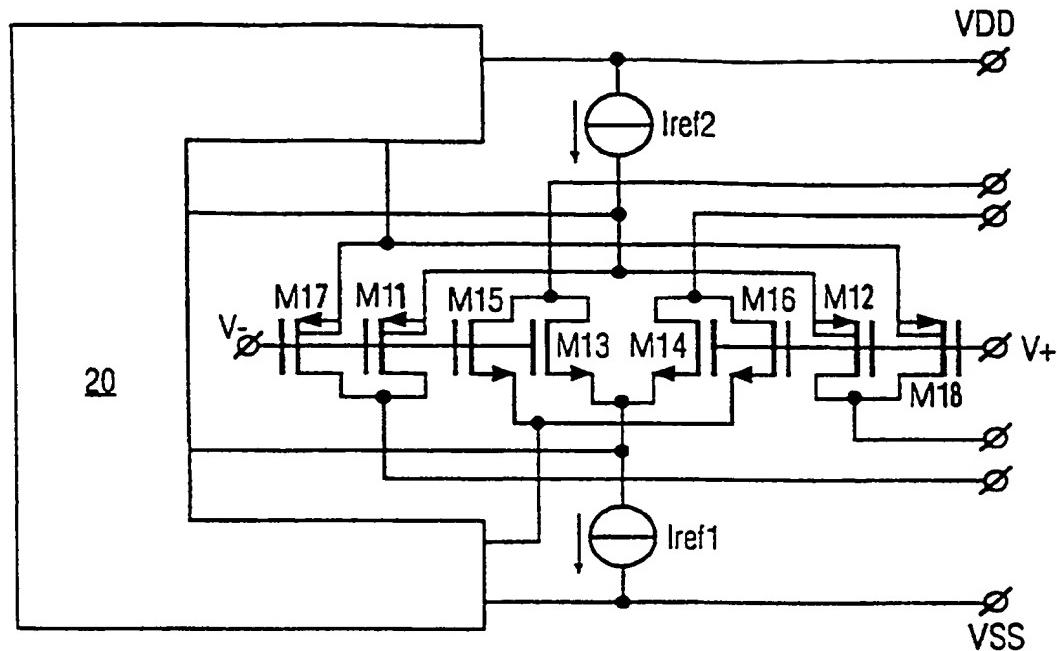


FIG. 2A

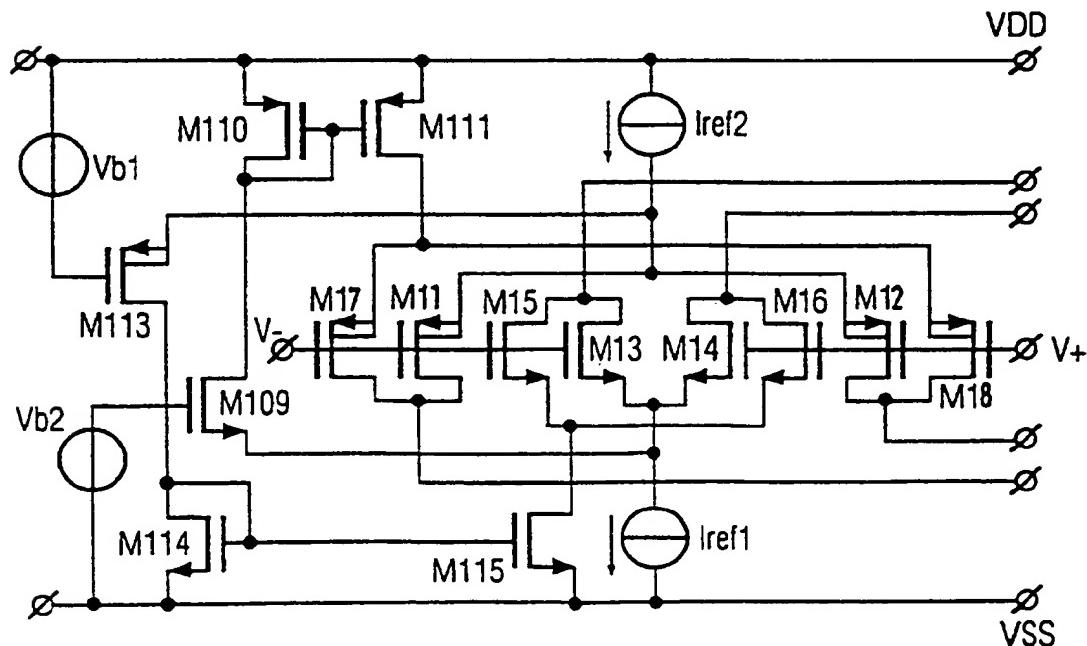


FIG. 2B

3/3

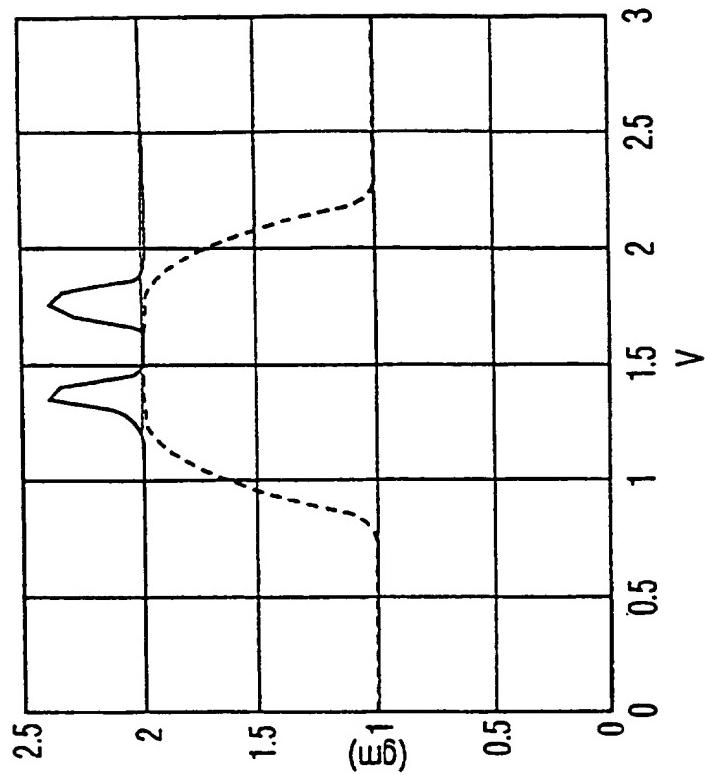


FIG. 3B

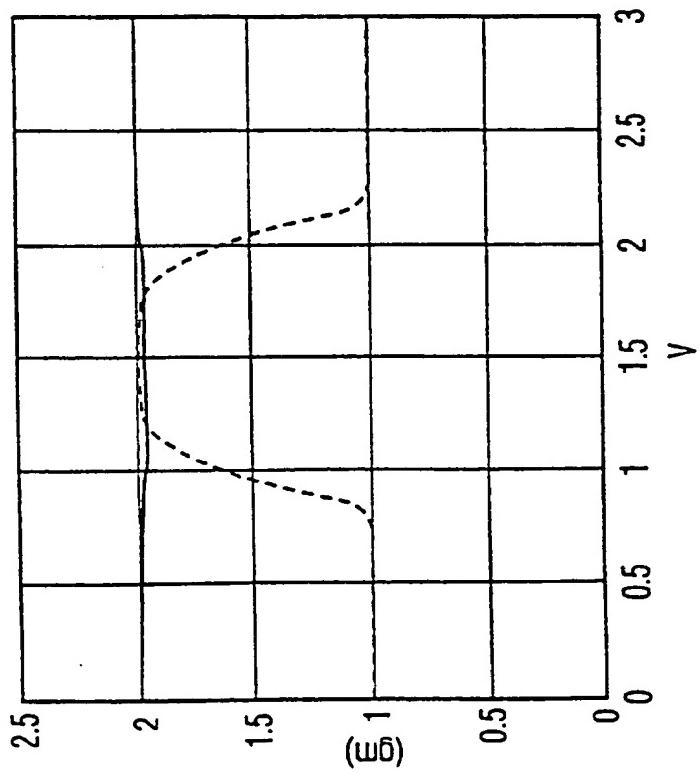


FIG. 3A